CLAIM AMENDMENTS

1. (Currently Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion, and the first single-piece housing portion is not integral with the second single-piece housing portion;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the first single-piece housing portion contacts the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

2. (Previously Presented) The device of claim 1, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

3. (Previously Presented) The device of claim 1, wherein the first single-piece housing portion contacts the lower surface.

4. (Previously Presented) The device of claim 1, wherein the insulative housing consists of the first and second single-piece housing portions.

5. (Original) The device of claim 1, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

6. (Original) The device of claim 1, wherein the terminal is a plated metal.

7. (Original) The device of claim 1, wherein the terminal is within a periphery of the chip, and the lead is outside the periphery of the chip.

8. (Original) The device of claim 1, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

9. (Original) The device of claim 1, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

10. (Original) The device of claim 1, wherein the device is devoid of wire bonds, TAB leads and solder joints.

11. (Currently Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing consists of a first single-piece housing portion and a second single-piece housing portion, and the first single-piece housing portion is not integral with the second single-piece housing portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the first single-piece housing portion contacts the lower surface and the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

12. (Currently Amended) The device of claim 11, wherein the second~~first~~ single-piece housing portion is farther from the top surface than the lower surface is from the top surface.

13. (Previously Presented) The device of claim 11, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

14. (Original) The device of claim 13, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

15. (Previously Presented) The device of claim 11, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

16. (Previously Presented) The device of claim 11, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the lead and the second surface provides a portion of the bottom surface.

17. (Original) The device of claim 11, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, and the lead is outside the periphery of the chip.

18. (Original) The device of claim 11, wherein the terminal is integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

19. (Original) The device of claim 11, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

20. (Original) The device of claim 11, wherein the device is devoid of wire bonds, TAB leads and solder joints.

21. (Original) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

22. (Currently Amended) The device of claim 21, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced

from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion.

23. (Original) The device of claim 22, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

24. (Original) The device of claim 23, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

25. (Original) The device of claim 22, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

26. (Original) The device of claim 21, wherein the peripheral portion of the bottom surface protrudes a first distance below the central portion of the bottom surface, the terminal protrudes a second distance below the central portion of the bottom surface, and the first distance is greater than the second distance.

27. (Original) The device of claim 21, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

28. (Original) The device of claim 21, wherein the terminal is within a periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

29. (Original) The device of claim 21, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the

central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

30. (Original) The device of claim 21, wherein the device is devoid of wire bonds, TAB leads and solder joints.

31. (Previously Presented) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad, wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance; and

a lead that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

32. (Currently Amended) The device of claim 31, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece

housing portion and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion.

33. (Original) The device of claim 32, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

34. (Original) The device of claim 33, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

35. (Original) The device of claim 32, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

36. (Original) The device of claim 31, wherein the first distance is about twice the second distance.

37. (Original) The device of claim 31, wherein the peripheral portion of the bottom surface is integral with the side surfaces and non-integral with the central portion of the bottom surface.

38. (Original) The device of claim 31, wherein the terminal is within a periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

39. (Original) The device of claim 31, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

40. (Original) The device of claim 31, wherein the device is devoid of wire bonds, TAB leads and solder joints.

41. (Currently Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

42. (Currently Amended) The device of claim 41, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface~~insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal~~.

43. (Original) The device of claim 42, wherein the first single-piece housing portion contacts the lower surface.

44. (Original) The device of claim 42, wherein the insulative housing consists of the first and second single-piece housing portions.

45. (Original) The device of claim 41, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

46. (Original) The device of claim 41, wherein the terminal is a plated metal.

47. (Original) The device of claim 41, wherein the terminal is within a periphery of the chip, and the lead is outside the periphery of the chip.

48. (Original) The device of claim 41, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

49. (Original) The device of claim 41, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

50. (Original) The device of claim 41, wherein the device is devoid of wire bonds, TAB leads and solder joints.

51. (Currently Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and

the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, and the upper surface faces towards the bottom surface and faces away from the top surface~~, and the insulative housing contacts the lower surface~~;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

52. (Currently Amended) The device of claim 51, wherein the second single-piece housing portion contacts the upper surface and is spaced from the lower surface~~insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal~~.

53. (Original) The device of claim 52, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

54. (Original) The device of claim 53, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

55. (Original) The device of claim 52, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

56. (Original) The device of claim 52, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the lead and the second surface provides a portion of the bottom surface.

57. (Original) The device of claim 51, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, and the lead is outside the periphery of the chip.

58. (Original) The device of claim 51, wherein the terminal is integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

59. (Original) The device of claim 51, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

60. (Original) The device of claim 51, wherein the device is devoid of wire bonds, TAB leads and solder joints.

61. (Previously Presented) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a routing line within the insulative housing that overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

62. (Currently Amended) The device of claim 61, wherein the insulative housing includes a first single-piece housing portion that contacts the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion.

63. (Previously Presented) The device of claim 62, wherein the first single-piece housing portion contacts the lower surface.

64. (Previously Presented) The device of claim 62, wherein the insulative housing consists of the first and second single-piece housing portions.

65. (Previously Presented) The device of claim 61, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

66. (Previously Presented) The device of claim 61, wherein the routing line and the terminal are a plated metal.

67. (Previously Presented) The device of claim 61, wherein the terminal is within a periphery of the chip, the routing line is within and outside the periphery of the chip, and the lead is outside the periphery of the chip.

68. (Previously Presented) The device of claim 61, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

69. (Previously Presented) The device of claim 61, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

70. (Previously Presented) The device of claim 61, wherein the device is devoid of wire bonds, TAB leads and solder joints.

71. (Previously Presented) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface, is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to

the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

72. (Currently Amended) The device of claim 71, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion.

73. (Previously Presented) The device of claim 72, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

74. (Previously Presented) The device of claim 73, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

75. (Previously Presented) The device of claim 72, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

76. (Previously Presented) The device of claim 72, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the routing line and the second surface provides a portion of the bottom surface.

77. (Previously Presented) The device of claim 71, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, the routing line is within and outside the periphery of the chip, and the lead is outside the periphery of the chip.

78. (Previously Presented) The device of claim 71, wherein the routing line is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

79. (Previously Presented) The device of claim 71, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

80. (Previously Presented) The device of claim 71, wherein the device is devoid of wire bonds, TAB leads and solder joints.

81. (Previously Presented) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from the side surfaces and is electrically connected to the pad; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one

another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

82. (Currently Amended) The device of claim 81, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion.

83. (Previously Presented) The device of claim 82, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

84. (Previously Presented) The device of claim 83, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

85. (Previously Presented) The device of claim 82, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

86. (Previously Presented) The device of claim 81, wherein the peripheral portion of the bottom surface protrudes a first distance below the central portion of the bottom surface, the terminal protrudes a second distance below the central portion of the bottom surface, and the first distance is greater than the second distance.

87. (Previously Presented) The device of claim 81, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

88. (Previously Presented) The device of claim 81, wherein the terminal is within a periphery of the chip, the routing line is within and outside the periphery of the chip, the lead is outside the periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

89. (Previously Presented) The device of claim 81, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

90. (Previously Presented) The device of claim 81, wherein the device is devoid of wire bonds, TAB leads and solder joints.

91. (Previously Presented) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from

the side surfaces and is electrically connected to the pad, wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

92. (Currently Amended) The device of claim 91, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion.

93. (Previously Presented) The device of claim 92, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

94. (Previously Presented) The device of claim 93, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

95. (Previously Presented) The device of claim 92, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

96. (Previously Presented) The device of claim 91, wherein the first distance is about twice the second distance.

97. (Previously Presented) The device of claim 91, wherein the peripheral portion of the bottom surface is integral with the side surfaces and non-integral with the central portion of the bottom surface.

98. (Previously Presented) The device of claim 91, wherein the terminal is within a periphery of the chip, the routing line is within and outside the periphery of the chip, the lead is outside the periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

99. (Previously Presented) The device of claim 91, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

100. (Previously Presented) The device of claim 91, wherein the device is devoid of wire bonds, TAB leads and solder joints.

101. (Currently Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that extends into the insulative

housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

102. (Currently Amended) The device of claim 101, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface~~insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal~~.

103. (Previously Presented) The device of claim 102, wherein the first single-piece housing portion contacts the lower surface.

104. (Previously Presented) The device of claim 102, wherein the insulative housing consists of the first and second single-piece housing portions.

105. (Previously Presented) The device of claim 101, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

106. (Previously Presented) The device of claim 101, wherein the terminal is within a periphery of the chip, and the lead is outside the periphery of the chip.

107. (Previously Presented) The device of claim 101, wherein the terminal is integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

108. (Previously Presented) The device of claim 101, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

109. (Previously Presented) The device of claim 101, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

110. (Previously Presented) The device of claim 101, wherein the device is devoid of wire bonds, TAB leads and solder joints.

111. (Currently Amended) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal, and the first single-piece housing portion is not integral with the second single-piece housing portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, and the upper surface faces towards the bottom surface and faces away from the top surface~~, and the insulative housing contacts the lower surface~~;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

112. (Currently Amended) The device of claim 111, wherein the second single-piece housing portion contacts the upper surface and is spaced from the lower surface~~insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal~~.

113. (Previously Presented) The device of claim 112, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

114. (Previously Presented) The device of claim 113, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

115. (Previously Presented) The device of claim 112, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

116. (Previously Presented) The device of claim 112, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the lead and the second surface provides a portion of the bottom surface.

117. (Previously Presented) The device of claim 111, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, and the lead is outside the periphery of the chip.

118. (Previously Presented) The device of claim 111, wherein the terminal is integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

119. (Previously Presented) The device of claim 111, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

120. (Previously Presented) The device of claim 111, wherein the device is devoid of wire bonds, TAB leads and solder joints.